



e-ISSN: 2278-8875  
p-ISSN: 2320-3765

# International Journal of Advanced Research

in Electrical, Electronics and Instrumentation Engineering

Volume 15, Issue 5, May 2026

**ISSN** INTERNATIONAL  
STANDARD  
SERIAL  
NUMBER  
INDIA

Impact Factor: 9.867

9940 572 462

6381 907 438

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# Design & Verification of AHB-Lite Based Memory Controller

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**ABSTRACT:** The Advanced High-performance Bus Lite (AHB-Lite) protocol is widely used in modern System-on-Chip (SoC) architectures for high-speed communication between processors, memory modules, and peripheral devices. This paper presents the design and verification of an AHB-Lite compliant slave memory controller using SystemVerilog and Universal Verification Methodology (UVM). The proposed design supports single and burst read/write transactions, multiple transfer sizes, and proper response generation through HREADY and HRESP signals. A finite state machine (FSM)-based architecture is implemented to manage address decoding, data transfer, and protocol synchronization. A reusable UVM verification environment consisting of sequencer, driver, monitor, scoreboard, and agent is developed to validate the functionality of the controller. Various test scenarios including single transfer, burst transfer, wrapping burst, back-to-back operations, and invalid address conditions are verified successfully. Simulation results demonstrate correct protocol compliance, reliable memory operation, and robust error handling suitable for SoC applications.

## I. INTRODUCTION

Modern SoC designs integrate processors, memories, and peripherals onto a single chip, requiring efficient communication protocols for reliable operation. AMBA AHB-Lite protocol developed by ARM provides high-speed pipelined communication suitable for embedded systems and memory subsystems. This work focuses on the design and verification of an AHB-Lite based slave memory controller. The controller supports read/write operations, burst transactions, and multiple transfer sizes while maintaining protocol compliance. A UVM-based verification environment is developed to ensure correctness under different operating scenarios.

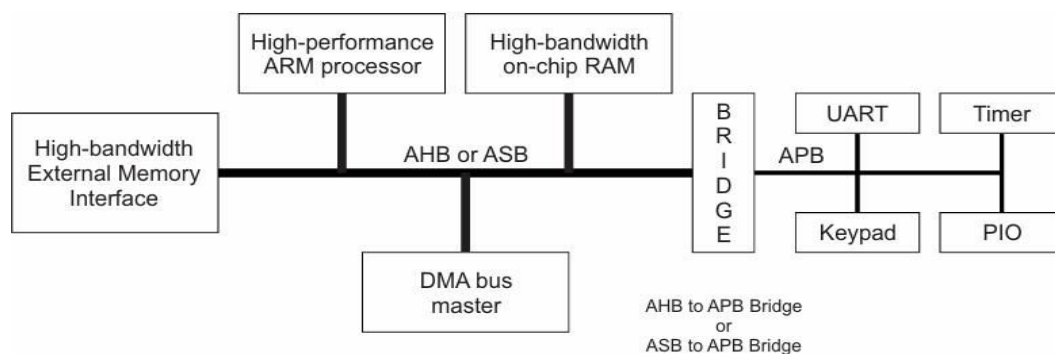


Fig.1 A Typical AMBA System

The fig.1 illustrates a typical AMBA-based System-on-Chip (SoC) architecture, where the AHB (Advanced High-performance Bus) acts as the main high-speed communication backbone. High-performance components such as the ARM processor, on-chip RAM, external memory interface, and DMA controller are connected directly to the AHB bus, enabling fast data transfer and efficient system performance.



II. LITERATURE SURVEY

Several researchers have proposed AHB and AHB-Lite based memory architectures for high-speed SoC applications. Previous works mainly focused on burst handling, memory access optimization, and protocol verification using UVM methodologies.

- Anila Kommineni et al. proposed an AMBA AHB-Lite memory controller supporting burst operations and SystemVerilog verification.
- M. Saravanan et al. implemented a 16/32-bit RAM using AHB protocol for embedded applications.
- B. Gamboa et al. developed a UVM-based verification framework for AHB-Lite to AXI bridge communication.

These works provided the foundation for the proposed AHB-Lite memory controller and reusable verification environment.

III. PROPOSED SYSTEM

The proposed system consists of an AHB-Lite slave memory module implemented using SystemVerilog RTL design. The design includes:

- 2 KB memory array
  - FSM-based transaction controller
  - Address decoding logic
  - Read/write operation handling
  - Burst transfer support
  - HREADY and HRESP response generation
- The memory controller supports:
- SINGLE transfer
  - INCR burst
  - WRAP burst
  - Byte, Halfword, and Word transfers

This fig.2 shows the architecture of an AHB Slave Memory system used for SoC communication. The AHB interface receives signals like HADDR, HTRANS, HWRITE, HBURST, HSIZE, and HWDATA from the master and sends them to the control and decoding blocks. The decoder identifies the transfer type and operation, while the FSM controller manages states such as IDLE, READ, WRITE, and RESPONSE. The design includes read/write data paths, address generation for burst transfers, and a 2 KB memory array for data storage. Finally, the response logic generates HRDATA, HREADY, and HRESP signals to ensure proper and reliable memory communication.

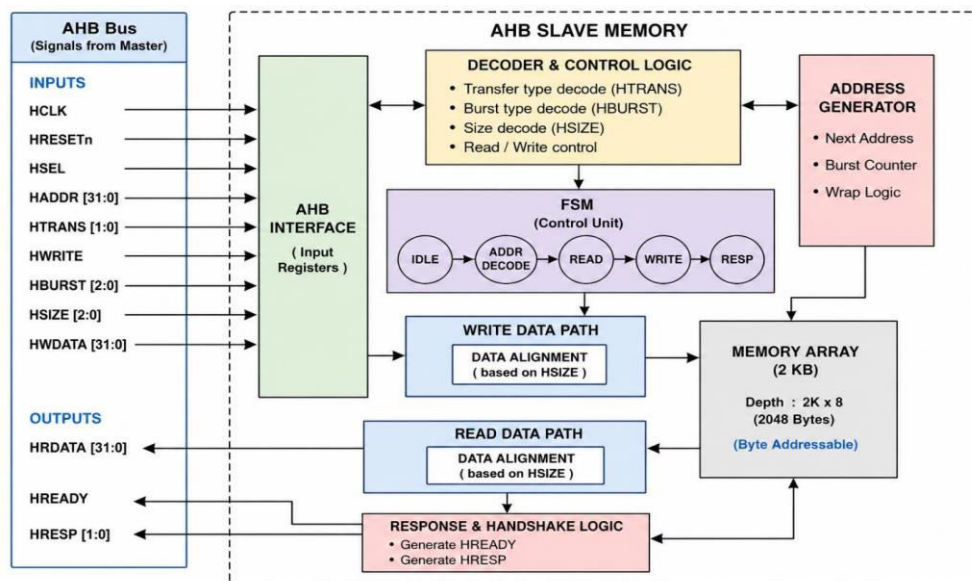


Fig.2 Block Diagram of AHB Slave Memory



IV. AHB-LITE ARCHITECTURE

The AHB slave communicates with the master through a set of **well-defined control, address, and data signals**. These signals enable proper synchronization, data transfer, and response handling between the master (testbench) and the slave (2 KB memory). Based on these inputs, the slave performs read/write operations and generates appropriate outputs.

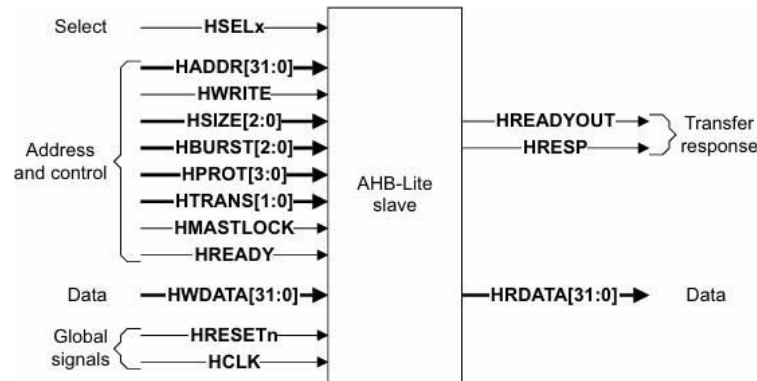


Fig.3 Slave Interface

Table 1 AHB Signals

Signal	Direction	Description
HCLK	Input	System clock for all AHB operations
HRESETn	Input	Active-low reset signal
HSEL	Input	Slave select signal
HADDR	Input	Address bus for memory access
HWRITE	Input	Indicates read (0) or write (1) operation
HTRANS	Input	Transfer type (IDLE, NON-SEQ, SEQ)
HBURST	Input	Burst type (SINGLE, INCR, WRAP, etc.)
HSIZE	Input	Transfer size (byte, halfword, word)
HWDATA	Input	Write data bus from master
HRDATA	Output	Read data bus to master
HREADY	Output	Indicates transfer completion
HRESP	Output	Response signal (OKAY, ERROR)

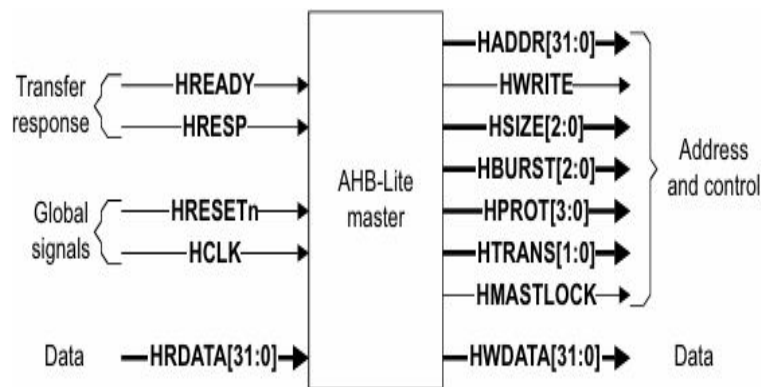


Fig.4 Master Interface



Table 2 Transfer Types

HTRANS[1:0]	Transfer Type	Description
00	IDLE	Indicates that no data transfer is required. The bus remains inactive during this cycle.
01	BUSY	Used by the master to insert wait states during burst transfers while maintaining control of the bus. No valid data transfer occurs.
10	NONSEQ	Represents the first transfer of a burst or a single transfer. The address is unrelated to the previous transfer.
11	SEQ	Indicates that the current transfer is part of a burst sequence and the address is related to the previous transfer.

### Burst Transfer Operation in AHB-Lite

The implemented AHB-Lite memory controller supports both incrementing and wrapping burst transfers. During burst operation:

- The first transfer always starts with HTRANS = NONSEQ
- Remaining transfers use HTRANS = SEQ
- Address progression depends on the selected burst type (HBURST)
- Wrapping bursts automatically wrap the address at predefined boundaries

This mechanism improves bus throughput and enables efficient high-speed memory access in System-on-Chip (SoC) architectures

## V. UVM VERIFICATION ENVIRONMENT

The verification environment is developed using UVM methodology. The testbench includes:

- Sequence
- Sequencer
- Driver
- Monitor
- Scoreboard
- Agent
- Environment
- Reporter

The figure 5 shows the UVM-based verification architecture for the AHB slave memory design. The testbench includes components like sequence, sequencer, driver, monitor, scoreboard, and reporter. The sequence generates different AHB transactions such as read, write, burst, reset, and invalid address operations, which are sent to the DUT through the driver. The monitor observes all bus activities and sends the data to the scoreboard for checking. The DUT consists of an AHB slave memory, control logic, FSM controller, read/write paths, and a 2 KB memory array. The control logic decodes signals like HTRANS, HBURST, and HSIZE, while the FSM controls states such as IDLE, READ, WRITE, and RESPONSE. The scoreboard verifies outputs like HRDATA, HREADY, and HRESP, and the reporter logs simulation results and errors, making the verification process reliable and automated.

The UVM environment generates different AHB transactions and verifies DUT behavior through automated checking mechanisms.

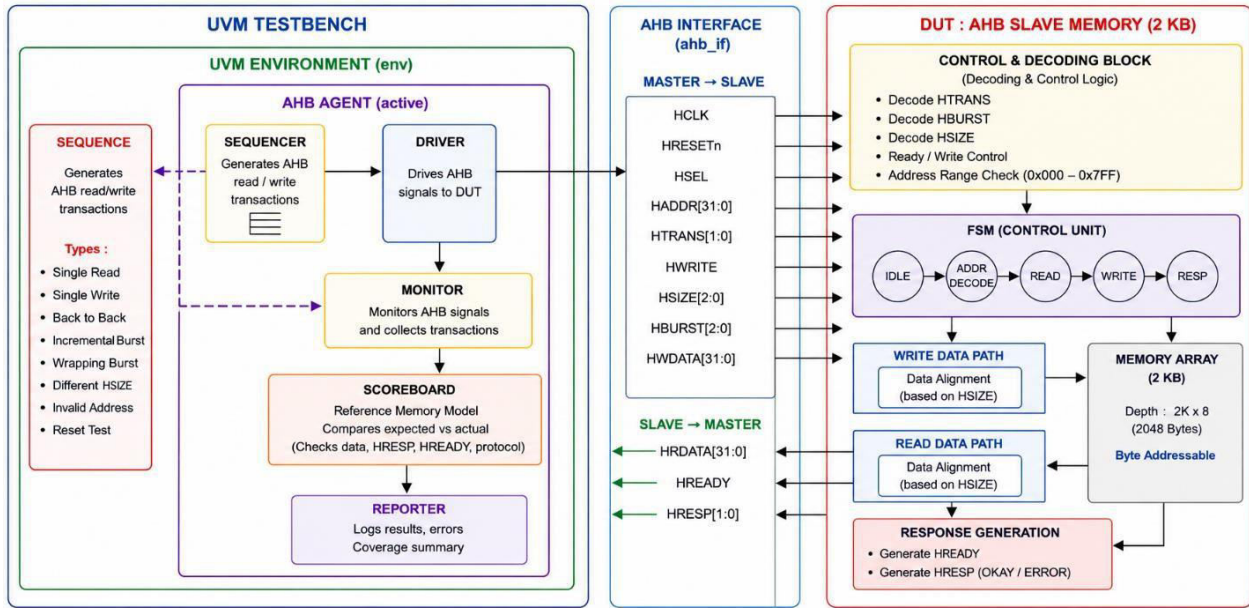


Fig. 5 Block Diagram of UVM Testbench Architecture for AHB Slave Memory

VI. RESULTS AND DISCUSSION

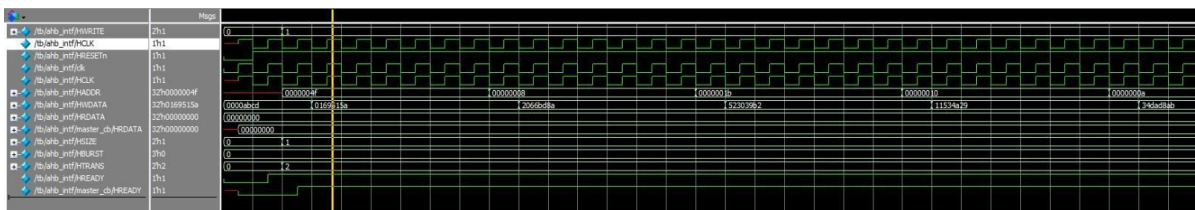
Simulation results confirm correct implementation of the AHB-Lite protocol. The DUT successfully performs read/write operations and burst transfers without protocol violations.

Key observations:

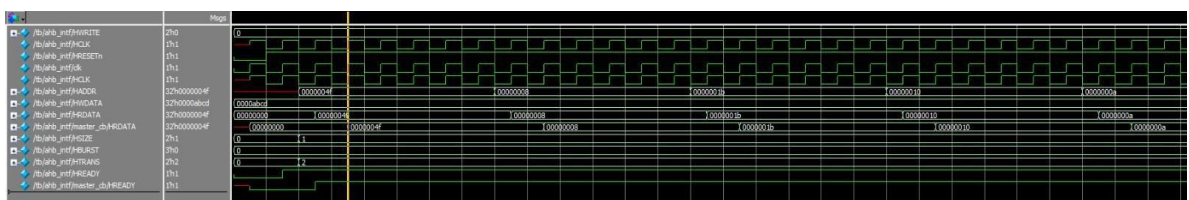
- Correct pipelined operation
- Accurate burst address handling
- Proper HREADY and HRESP generation
- Successful error detection for invalid addresses
- No scoreboard mismatches during verification

Test Scenarios

1. Single Write: HTRANS=2'b01, HBURST=3'b000, HSIZE=3'b001,HWRITE=1

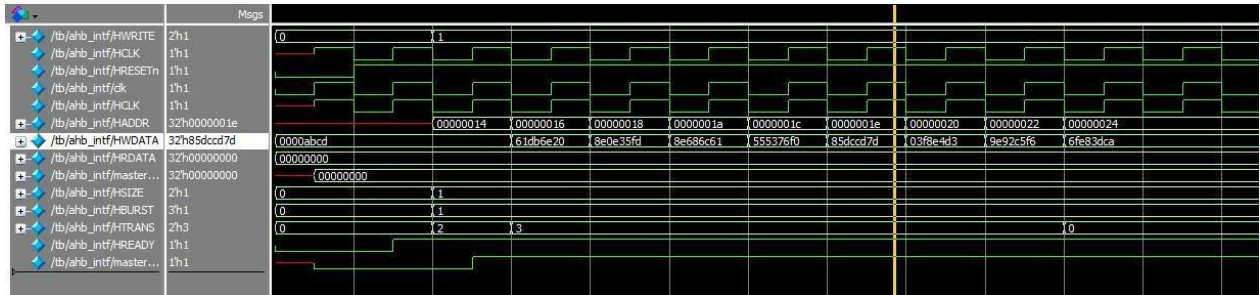


2. Single Read: HTRANS=2'b10, HBURST=3'b000, HSIZE=3'b001,HWRITE=0

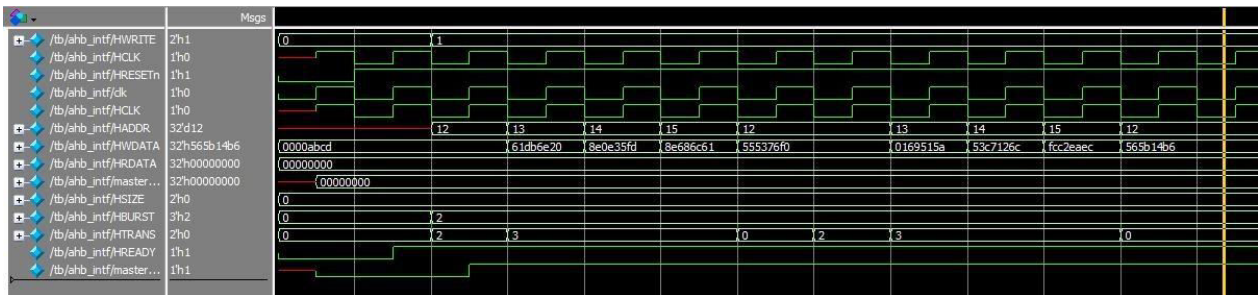




**3. INCR BURST: HBURST=3'b001, HSIZE=3'b010, INCR BURST, address increments by 4**



**4. WRAP4: HBURST=3'b010, HSIZE=3'b000, WRAP4, 4 BEAT WRAPPING BURST**



The UVM-based environment improved verification efficiency and reusability.

**VII. ADVANTAGES**

- High-speed data transfer
- Efficient burst handling
- Modular RTL architecture
- Reusable UVM verification environment
- Reliable protocol compliance
- Scalable for SoC integration

**VIII. APPLICATIONS**

- SoC memory subsystems
- Embedded systems
- DMA communication
- Processor-memory interface
- High-speed digital systems
- Networking applications

**IX. CONCLUSION**

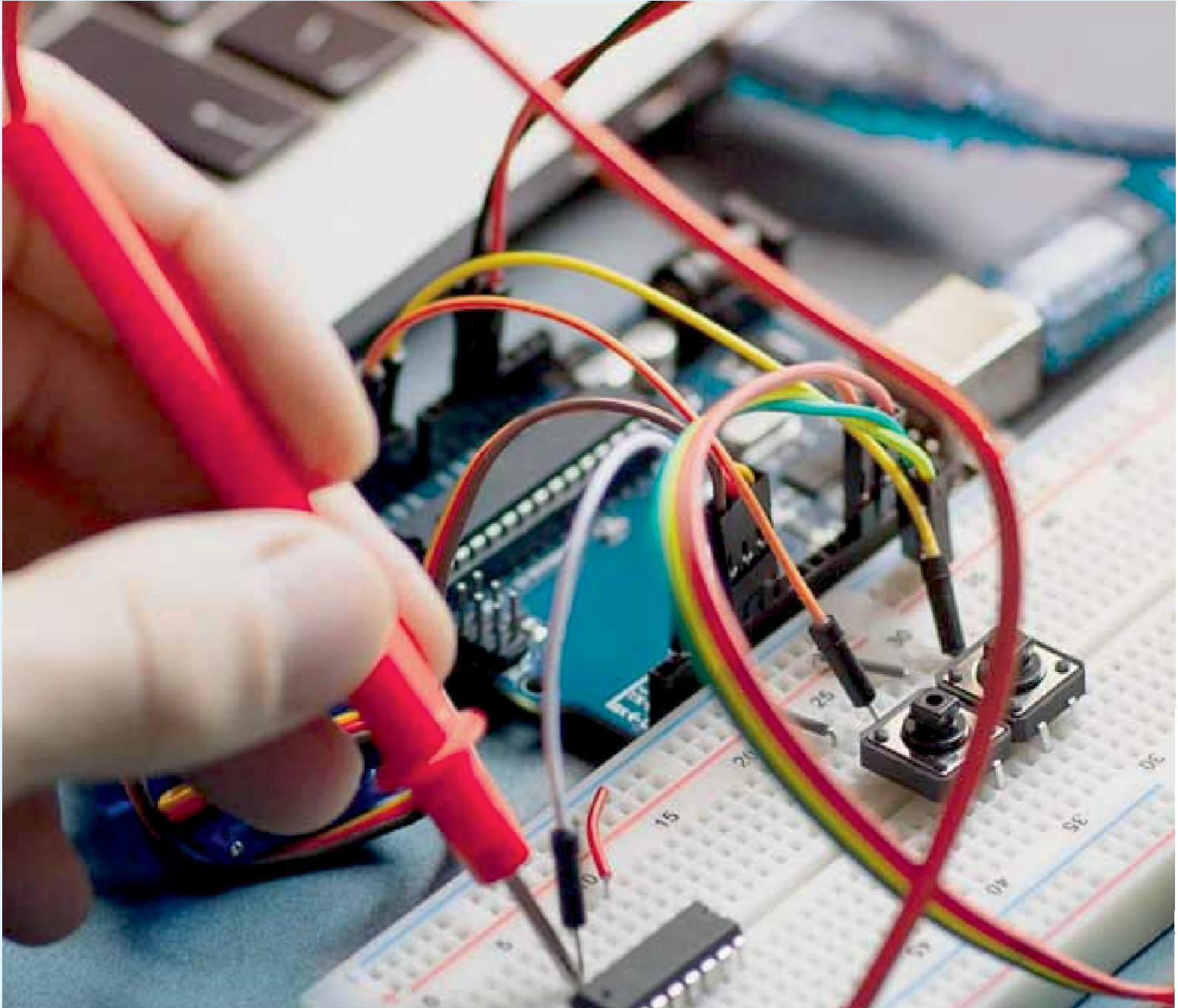
An AHB-Lite based slave memory controller was successfully designed and verified using SystemVerilog and UVM methodology. The design supports burst transfers, multiple data sizes, and protocol-compliant memory transactions. The developed UVM environment verified the functionality under different test conditions and confirmed reliable operation suitable for modern SoC applications.

Future enhancements may include multi-master support, wait-state insertion, assertion-based verification, and AXI bridge integration.



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